What is claimed is:

1. A programmable counter comprising:

multiple latches for providing a count output;

a first circuit for providing a start count value coupled to said latches;

a second circuit for providing a stop count value coupled to said latches;

a third circuit coupled to the latches for providing a maximum count value to said latches; and,

a compare circuit coupled to the second circuit and the latches for comparing the count with the stop count.

2. The programmable counter of claim 1 wherein the third circuit comprises a toggle controller for receiving the count value and selectively providing toggle control signals to inputs of the latches.

3. The programmable counter of claim 2 wherein the toggle controller is provided the count from the latches and further provides a toggle control signal to each latch causing each latch to generate a 0 bit count based on a predetermined rollover value of said count.

4. The programmable counter of claim 3 wherein the rollover value of said count is decimal 111.

5. The programmable counter of claim 2 wherein the latches further comprise circuitry for resetting the value of the count to the start value upon reaching the stop count.

6. The programmable counter of claim 1 wherein the latches further comprise circuitry for resetting the value of the count to the start value upon reaching the stop count.

7. The programmable counter of claim 1 wherein each latch corresponds to one bit of a 7-bit count value.

8. A programmable counter comprising:

multiple latches for providing a count output;

a first circuit for providing a start count value coupled to said latches;

a second circuit for providing a stop count value coupled to said latches;

a compare circuit coupled to the second circuit and the latches for comparing the count with the stop count to provide a match indication causing the latches to be reset.

9. A method of counting implemented by digital logic circuitry comprising the following steps:

limiting the count to a maximum count value;

providing a start count value;

providing a stop count value which may be less than the start count value;

counting sequentially from said start count value;

resetting the count to 0 upon reaching the maximum count value; and

continuing to count from 0 until the stop count value is reached.